FERRANTI PEGASUS COMPUTER

VOLUME 5

PACKAGES

FERRANTI LTD.
Head Office: HOLLINWOOD, LANCASHIRE,
ENGLAND

COMPUTER DEPARTMENT

Offices and Works:

WEST GORTON WORKS
THOMAS STREET
WEST GORTON
MANCHESTER, 12

Tel: EASt 1301

London Computer Centre:

21, PORTLAND PLACE,
LONDON W.1

Tel: LANgham 9211

Copy No. 127

SUMMARY

This volume deals with packages used in Pegasus installations. Packaged circuits have been designed to perform logical operations on a 3μ sec. positive-going digit pulse; to generate and control additional 'clock' and 'reset' waveforms required by the system; to write on, and read from, a selected track on a drum backing store; to write on, and read from, magnetic tape; and to store information in immediate-access and medium-access sonic lines.

HT supplies at +300V, +200V and -150V are required, and the packages have been designed to operate satisfactorily on HT margins of +5% and -10%. There is a general requirement for bias supplies at +13V, -10V and -20V, and a centre-tapped AC heater supply of ±6.3V is necessary. The components used on the packages have been standardised as far as possible, and there is some standardisation too in the use of pins on the package plugs. The pin connections are tabulated in detail on the frontispiece to Volume 5a.

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CHAPTER I

COMPUTING PACKAGES

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CHAPTER I

COMPUTING PACKAGES

1. The packages described in this chapter incorporate circuits that perform the logical AND and OR operations and the operation of inversion; they also include digit delay circuits, delay lines and cathode followers (which are necessary when the loading is high on a particular waveform). They are built up of convenient combinations of simple circuit elements, and most packages contain two or more identical, or closely similar, circuits.

2. The basic waveforms are shown in fig. 1.1. All timing is related to 'clock', a 3μ sec. square wave of unity mark-space ratio and nominal amplitude 12V, with its base level at -10V. This is used in conjunction with 'reset', a negative-going pulse of width 0.6μ sec. and amplitude at least 38V, its falling edge coincident with the falling edge of 'clock'. The digit pulse itself is generated in the digit delay circuit, which appears on package types 1, 2 and 6. This circuit accepts a 'clocked' pulse (i.e. the result of an AND operation between a digit pulse and 'clock') and feeds out a digit pulse with its front edge defined by the back edge of the next 'reset' pulse. A digit pulse thus starts its life with its leading edge about $3/4\ \mu$ sec. ahead of 'clock'; its peak level at this stage is about +20V, and its base level is, as always, at -10V.

3. As all digit pulses are 'clocked up' on entering delays, quite a large amount of pulse distortion can be tolerated. In particular, the digit pulse can be retarded by stray circuit capacitance by more than a quarter of its own width before the operation of the machine is impaired. Fig. 1.1 shows some effects of logical operations between digit-pulse trains with slightly different timing; any 'spikes' formed in the process are eliminated, as shown, by subsequent 'clocking-up' operations.

4. The gaps between succeeding pulses are narrow, and, owing to normal wiring capacitance, the signal level does not fall to the minimum between adjacent pulses. Consequently direct coupling must be used between the elements, rather than AC coupling with DC restoration. The 'merging' of adjacent pulses does not affect the logical operation of the circuits, of course, as only the part of the waveform 'overlapped' by 'clock' has any significance. In fact adjacent pulses in the output of the inverter (package type 3) are completely merged, a series of 'ones' being represented by +14V to +17V DC according to the loading.

5. The OR operation is, of course, equivalent to a simple 'mixing' of pulse waveforms. As the same waveform will usually enter into several logical operations, however, blocking crystals may have to be used when waveforms are mixed. An OR-gate-cathode-follower combination with four crystals is provided (package type 8); but the majority of the OR gates normally required can be made up from components on the other packages as most of the logical elements have, as well as a direct output, a 'mix' output through

a crystal. Notice that signals fed to the direct-output point from an outside source will also appear at the 'mix' output.

6. An OR gate presents a relatively low impedance to its input; fig. 1.2 shows a typical crystal OR gate to indicate loading demands. The bleed resistor down to -150V ensures that an OR gate with all its inputs 'down' can 'hold down' a succeeding AND gate; if the bleed resistor were not there, the output of the OR gate would be connected to -10V only through the high back resistances of the crystals. The bleed resistor should have a resistance as high as possible to minimise the loading on the inputs: all packages with 'mix' outputs provide a choice of bleed resistance, the resistor or resistors being connected in via the back wiring. If a single OR input is 'up' while the rest are 'down', the conducting crystal may have to pass as much as 7 mA; the consequent drop of one or two volts across the crystal must be allowed for in the logical design (see paragraph 10).

7. The entries to most of the logical elements are AND gates, gates with two, three or four signal inputs being provided. Fig. 1.2 shows a typical three-input gate in three different conditions. (Loading after the gate, e.g. due to grid resistors, is omitted here for simplicity.) Bleed is to +200V, so the output level is just above the lowest input level; consequently the output is 'down' as long as at least one of the inputs is 'down', and the output of an 'open' AND gate is just above the level of the weakest input. The 'hold-down' current for an AND gate is supplied by those inputs that are 'down'; consequently each input source, when it alone is 'down', must supply enough current to provide the correct potential drop across the bleed resistor and across the back-conduction resistance of the other crystals.

8. The output stage of most of the logical elements is a cathode-follower. When this is driving an OR gate, the 'pull-up' current is supplied through the valve; the cathode-load resistance must then be fairly high to keep the current in the valve as low as possible. On the other hand, when the cathode-follower is driving one or more AND gates, the cathode resistance must be low enough to take the sum of the 'hold down' currents as well as the residual valve current in the 'down' condition. The packages provide a choice of cathode resistors, already tied to the -150V line, that can be connected into circuit by the back wiring. All cathode-follower outputs are caught negatively at -10V by crystal diodes tied to the bias line.

LOGICAL-DESIGN RULES

9. Lines, delays and inverters restore the levels of digit waveforms: lines and delays, but not inverters, also standardise the timing of digit pulses. The logical designer will very seldom be concerned with the problem of pulse 'slip', as the logic is unlikely to be such that the signal level can be restored often enough by inverters to allow the edge of the digit waveform to fall behind 'clock'. The main problems of detailed design are therefore:

(i) to ensure that the 'up' level of the digit pulse does not fall below +1V;
(ii) to choose cathode-follower tail resistors that are suited to the loading imposed by driven gates.

Levels

10. The 'up' level of the output of a nickel line, delay or inverter is, even under the worst conditions of supply and circuit tolerances, and with valves on the borderline of rejection, well above +13V. A cathode-follower with a poor valve can cause a drop in level up to 5V: an OR gate made up from 'mix' outputs can, under the worst conditions, cause a drop in level of about 2V. A maximum of two cathode-followers and one 'mix' is therefore permissible between any two level-restoring devices (line, delay or inverter). Levels are referred to by Greek letters: the standard level is α; a cathode-follower reduces this to β and a further cathode-follower to γ; the effect of a 'mix' is to add a 'minus' to the symbol, so that the minimum permissible level is γ-. Note that a cathode-follower combined with a gate is treated as a cathode-follower alone, but that the lowest level of the signals entering a gate is taken as fixing the output. Fig. 1.3 shows two permissible examples of logical design and one arrangement that might be expected to give trouble under extreme conditions.

Loading

11. As an illustration of the type of reasoning required in choosing cathode-follower tail resistors, consider the circuit shown in fig. 1.3, in which the output from cathode-follower V1 enters into AND operations with waveforms A and B to control the grid potentials of valves V2 and V3. An upper limit is set on the tail resistance, R_t, by the fact that the potential across it must not be greater than 132.5V (allowing for a 5% tolerance on the negative HT supply) when the input to V1 is at the 'down' level. The current, i_t, through the tail resistor is made up from the standing current, i_1, in V1, which may not be completely cut off, the leakage currents, i_2 and i_5, through crystals D2 and D4, and the currents through the AND-bleed resistors less the currents through the grid-bias resistors, $(i_3 - i_4)$ and $(i_6 - i_7)$. These last two currents are referred to as 'bleeder currents'; they are to be calculated for an HT supply 5% above the nominal value, and the resistances must be assumed to be below the nominal values by 1% more than the stated tolerance. The back current through a crystal is taken as 0.25 mA. The standing current through the cathode-follower valve depends on the circuit containing it: it is usually one to two milliamps.

12. The lower limit to the value of tail resistance is set by the requirement that the valve current must not be too high when the input of V1 is 'up'. The loading should be adjusted so that the valve is capable of giving an output level α with no more than 10 mA of anode current; this will take care of any case in which it is required to give a lower level of output. The valve current drains away to -150V through the tail resistor, and to -10V owing to the inverse leakage of the cathode-catching crystal and the input crystals of those driven gates that are closed. Obviously, if all the driven gates are closed, a drop in signal level will not matter. The worst case occurs therefore when all the gates are closed except one; if there are n gates altogether, there will be n drain-away crystals (i.e. n-1 gating crystals and one cathode-catching crystal).

13. In calculating the minimum value of tail resistance for the 'up' condition of output, the worst conditions of circuit tolerance are considered, i.e. the negative line is assumed to be 5% below its nominal level and the tail resistance to be less than its nominal value by 1% more than the stated tolerance. This will give a value

of tail current greater than that calculated for the 'down' condition in the ratio of about 10:7. A simpler procedure, therefore, would be to assume the same values of tail resistance and PD, and hence of tail current, as were used in analysing the 'up' conditions, and to reduce all the other currents in the circuit in the ratio of 7:10. The maximum valve current can then be taken as 7 mA, and the back-conduction currents through the crystals as 0.17 mA.

14. All cathode-followers are provided with a fixed tail resistance with a 5% tolerance. The packages also carry loose loads, already tied to the -150V line, which can be connected in parallel with the fixed loads by suitable back-wiring connections. Four load values are used; these are designated by the letters *a*, *b*, *c* and *d* as follows:-

	LOAD	CURRENT ALLOWANCE
a	120K	1.0 mA
b	75K	1.7 mA
c	51K	2.5 mA
d	Two 75K in parallel	3.3 mA

Letters indicating any *loose* loads used are marked on the logical working diagrams.

15. The general procedure for choosing suitable loose loads is given below.

A. Determine a lower limit for the tail current as follows:-

(i) Consider all driven gates, and find the maximum number of other inputs to these gates that can be 'up' at any one time when the output under consideration is 'down'. Allow 0.25 mA for each input.

(ii) Find the sum of the bleeder currents (current through bleed resistor less current through any grid resistor) for the driven gates.

(iii) Find the standing-current allowance in the cathode-follower giving the output under consideration.

(iv) Add together the currents found in *(i)*, *(ii)* and *(iii)*.

B. Determine an upper limit for the tail current as follows:-

(v) Allow 0.17 mA for each gate fed from the source under consideration.

(vi) Subtract the current found in *(v)* from 7 mA.

C. Using the table given in paragraph 14, select from the resistors available on the package a combination to give a current lying between the two limits. The currents in the table are calculated for the 'down' condition with the negative HT supply 5% smaller than its nominal value and with resistances greater than the nominal resistor values by 1% more than the stated tolerance. Back-wiring inter-connections should be as short as possible. If the calculated lower limit of current exceeds the calculated upper limit, supplementary cathode-followers must be used, provided that levels are high enough; otherwise the logical design must be revised.

'Mix' Outputs

16. Considerations affecting the choice of bleed resistor for the 'mix-output' type of OR gate are similar to those given above for the choice of tail resistor. In the 'down' condition, the current through the bleed resistor must be equal at least to the sum of the bleeder currents for all the driven gates, plus 0.25 mA crystal back current for each of the entries to these gates that can be 'up' while the 'mix' signal is 'down'. There should be an additional current allowance because of stray capacitance; this will depend on various factors such as lead lengths; but a value of 1.0 mA can be taken as a rough working rule. When one of the inputs to the 'mix' is 'up', the corresponding crystal is forward-conducting and the tail resistor and OR-bleed resistor are in parallel. An upper limit to the total current through these two resistors can be calculated by allowing 0.17 mA for each driven AND gate that can be 'closed' when the output under consideration is 'up', and a further 0.17 mA for each input to the 'mix' that can be 'down' at the same time. The total current so found is then subtracted from 7 mA as in B of paragraph 15. This procedure must be repeated for each of the elements feeding the 'mix'. Note that, in calculating a *lower* limit for the tail current in an element whose direct and 'mix' outputs are *both* in use, there must be an addition of 0.25 mA for back conduction through the 'mix' crystal, over and above the currents detailed in A of paragraph 15, to allow for the cases in which the 'mix' output is raised by one of its other inputs.

Exclusiveness

17. It is often possible to economise on the use of cathode-followers by taking the logical meaning of waveforms into consideration. For example the source of a waveform A that is gated once with waveform B and once with its inverse, ~B, will never have to hold both gates down together. Thus the lower limit of tail current in the source of A can be calculated as if A were connected to only one gate. Two gates must be considered in calculating the upper limit of current, or, more precisely, one gate and one catching crystal.

18. A common logical circuit is one in which AND gates are used to give the eight possible combinations of a waveform A or its inverse ~A with waveforms B or ~B and C or ~C. One, and only one, of these gates can be open at any one time, and three of the gating waveforms must always be 'up'. Hence the sources of the three waveforms that are 'down' must together absorb seven bleeder currents and nine back-conduction crystal currents. The tail currents can then be much smaller than would have been necessary had the gating waveforms been completely random. The total tail current may be shared equally between the sources of the waveforms that are 'down', or, if one waveform, A say, is fed to a gate extra to those already considered, its source may be arranged to supply a smaller share of the current. Incidentally, a reduction in the proportion of current supplied by the source of A implies in this arrangement a reduction in the proportion supplied by the source of ~A.

19. It is standard practice to connect one input of any unused element to -10V to reduce power consumption and heating. When only one of the two AND gates of a twin delay or line is used, one of the inputs to the unused gate must be connected to -10V, otherwise this gate will be permanently 'open'.

DIGIT DELAYS (TYPES 1 AND 2)

20. The digit delay unit accepts a clock-standardised digit pulse and generates a new pulse during the next digit-time. It is therefore often used as a pulse reshaper where a delay may not be logically necessary. Fig. 1.4 shows the basic delay circuit and typical waveforms at different points in the circuit during the digit sequence 01100. The circuit employs one 12AT7 double triode, of which one half is an amplifier and the other half a cathode-follower with its output caught negatively at -10V. The pulse is absorbed and re-formed by a network consisting of C1, C2, L and D1, the back edge of the new pulse being defined by the front edge of 'reset', a negative-going pulse about 0.6μ sec. wide running from +18V to between -20V and -25V, which is applied through an AND diode to the grid of the cathode-follower.

21. In the absence of clocked digits at the input grid, V1 is cut off; so its anode is at +200V. The grid of V2 is then maintained at a mean level just below -20V by the integration of successive reset pulses by C2. On the arrival of a 'clocked-up' digit, the operation of the circuit is as follows:-

(i) The anode of V1, and hence the junction of L and C1, drops by about 100V, and C1 starts to discharge through L and V1. The discharge of C1 is quite rapid, as damping is just below the critical value; while V1 is conducting, the potential across C falls by about 30V, and the current in L rises to about 8 mA.

(ii) At the end of the 'clocked-up' digit, the anode of V1 rises. At the same time the 'reset' level falls below -20V forcing the grid of V2 and, as D1 is now forward-conducting, the junction of L and C1 to follow its profile. Inductive inertia maintains the current in L, which now flows mainly through D2 to the 'reset' line; very little inductive energy is lost, however, as the potential across L is almost zero at this stage.

(iii) When 'reset' rises again to +18V, D2 presents a high impedance, and the whole of the current in L is diverted to charge C2. L and C2 form a ringing circuit; but the upward swing at the grid of V2 is caught at +18V by D2, any residual current in L being bled away to the 'reset' line. C2 now discharges slowly through the grid leak and through the back resistance of D1. The appearance of another clocked-up digit will, by reducing the potential at the diode of V1, accelerate the discharge; but in any case the potential at the grid of V2 falls by 2V at the most.

(iv) The next 'reset' pulse discharges C2 and restores the grid potential of V2 to about -20V, thus defining the end of the digit pulse. The positive excursion at the grid of V2 is reproduced at the cathode; but the negative portion is clipped by diode D3, to give the digit-pulse waveform a flat base level at -10V. The maximum 'up' level at the output is about +20V.

22. The full circuits of the twin-delay element (package type 1) and the single-delay element (package type 2) are shown in figs. 1.5 and 1.6 respectively. It will be noticed that diodes D1 and D2 consist of two type-CG10E crystals in series; this is

to reduce potential variations across C2 due to current drain through the back conductance at the 'up' level (D1) and the 'down' level (D2). Note that the regulation of the 'reset' supply must be very good, as the discharge of C2 gives a peak current of about 7 mA, to which must be added, immediately after an input digit, the current of about 8 mA through L.

Twin Delay (Type 1)

23. The twin delay incorporates two three-input AND gates with their outputs mixed and gated with 'clock'. Owing to the number of input terminals required, only two elements can be accommodated on the package, although there is room for three valves. The AND-gate bleed resistors are smaller than for the single delay (see fig. 1.6) because they must supply the 'lift' current for the OR gate. The 680K grid-leak resistor R2 is necessary to hold the input grid down against 'clock' when none of the inputs is positive; if R2 were open-circuited, the back conductance of the OR crystals and the 'clock' crystal would fix the grid potential during 'clock' too close to 'cut-on' for safety. Fig. 1.5 shows the circuit of one twin-delay element; pin and component numbers for element 1, and (in brackets) for element 2, of the package are shown on the figure. Fig. 1.7 shows the component layout and wiring of the whole package. Test sockets are provided at the direct and 'mix' outputs of the two elements.

24. Loading Data

(i) Standing current 1.0 mA.
(ii) Bleeder current 0.8 mA.
(this includes an allowance for leakage current through the clocking crystal).
(iii) Fixed load 1.0 mA.
(iv) Loose loads.

Pin number	Load value	
10	3.3 mA	Associated with first element on package.
15	1.7	
20	2.5 mA	Associated with second element on package.
17	1.7	
23	3.3	

N.B. If only one input is used, an allowance must be made for leakage through the input crystal when the gate is held down by 'clock'.

Single Delay (Type 2)

25. There are three single delays to a package, each being preceded by a four-input AND gate, of which one input is used for 'clock'. The gate is conventional and, as the loading is small, the bleed resistance is quite high. The circuit of fig. 1.6 shows pin and component numbers for element 1, element 2 (in round brackets) and

element 3 [in square brackets]. Fig. 1.8 shows the component layout and wiring. A test point is provided for each direct output and each 'mix' output.

26. Loading Data

(i) Standing current 1.0 mA.
(ii) Bleeder current 0.6 mA.
(iii) Fixed load 1.0 mA.
(iv) Loose loads.

Pin number	Load value	
7	1.7 mA	Associated with first
10	3.3	element on package.
17	1.7 mA	Associated with second
20	2.5	element on package.
26	1.7 mA	Associated with third
29	3.3	element on package.

N.B. If only one input is used, an allowance must be made for leakage through the input crystal when the gate is held down by 'clock'.

INVERTER (TYPE 3)

27. The inverter consists of a single inverting amplifier feeding a cathode-follower output stage. Because the digit waveform does not quite drop to the base level between consecutive pulses, and because the extent of the actual drop is not constant, the two stages in the inverter must be direct-coupled, rather than capacitor-coupled with DC restoration. Fig. 1.9 shows the inverter circuit. The delay imposed by the coupling network is reduced by the use of a 22pF coupling capacitor, and also by catching the signal in the negative direction to eliminate the delay in rise time that would follow a long negative excursion at the grid.

28. The 'bootstrap' connection of the catching crystals MR5 and MR4 ensures that they are never subjected to more than a few volts in the reverse direction, and that consequently the leakage current through them is always small. When the output is 'down', the cathode of the cathode-follower is caught at -10V by MR9; the junction of R6 and R7 is then very slightly below this, the cathode-follower being cut off by the potential drop across R7. As the junction of MR5 and MR6 is also at -10V (MR7 conducting), the current drain through the back conductance of the positive catch, MR5, is slight. When the output is 'up', the grid is caught at +13V by MR5 and MR6; the cathode is at +14V to +17V, according to load, so that the reverse potential across, and hence the current drain through, MR4 is small.

29. The HT supply to the inverting valve is 300V. This enables the upper level of output to be attained in spite of the relatively high resistance at R6 that is needed

to give a definite, sharp negative swing. The positive level of the output is +14V to +17V according to load. The inverter output is an α-level signal, i.e. it will still give a safe signal after attenuation by the design maximum of two cathode-follower stages and a 'mix', although it is slightly lower than the output of the delay elements. Consecutive pulses in the inverter are represented by a steady DC at the 'up' level. The gap between positive input pulses is reproduced as a very attenuated positive spike, which is well outside 'clock' and so has no effect on the logical operation of the system.

30. The entry to the inverter element is a three-input AND gate; it is similar to the gate preceding a single delay, except that the bleed resistance can be lower because of the reduced loading with only three inputs (no 'clock'). There are three inverter elements to a package; fig. 1.10 shows pin and component numbers for element 1, element 2 (in round brackets) and element 3 [in square brackets]. Test points are provided for each direct output and each 'mix' output. The component layout and wiring are shown in fig. 1.11.

31. Loading Data

(i) Standing current 1.0 mA
(ii) Bleeder current 0.7 mA
(iii) Fixed load 1.0 mA
(iv) Loose loads

Pin number	Load value	
7	1.7 mA	Associated with first
10	3.3	element on package.
17	1.7 mA	Associated with
20	2.5	second element
21	3.3	on package.
26	1.7 mA	Associated with third
29	3.3	element on package.

N.B. When the gate preceding an inverter is 'open', the grid of the valve is caught at about +2V by grid current, so that there can be up to 13V across the crystals. When there is only one input to the element, it is standard practice to use two crystals in parallel (providing a margin of safety); the drain-away current through them is then equivalent to that through a single crystal with the maximum digit-pulse peak-to-peak voltage across it. A current drain of 0.17 mA can then be allowed for the inverter gate, and a further 0.17 mA for the catching crystal at the driver cathode.

'AND' GATE (TYPE 4)

32. The circuit of the AND gate package is shown in fig. 1.11 and the layout in fig. 1.12. One two-input gate, two three-input gates and one four-input gate are

provided; each precedes a cathode-follower, of which all except the first have a 'mix' output as well as a direct output. Each cathode-follower uses one half of a 12AT7 double triode. Only two valves are used, the package arrangement being limited by the number of pins available on the connector and the conventions adopted for their use. The bleed resistors on the gates are low because of the current required by the grid-bias resistors. Test points are provided for the four direct outputs and the three 'mix' outputs.

33. Loading Data

(i) Standing current 2.0 mA
(ii) Bleeder current 0.8 mA
(iii) Fixed loads
(a) First element 5.8 mA
(b) Other elements 2.5 mA
(iv) Loose loads

Pin number	Load value	
9	1.0 mA	Associated with second element.
7	2.5	
20	2.5 mA	Associated with third element.
21	1.0	
25	3.3 mA	Associated with fourth element.

NICKEL LINE (TYPE 6)

34. A compression wave is induced at one end of a piece of nickel wire by magneto-striction. This wave travels down the wire at the velocity of sound in nickel, and is picked up at the remote end by virtue of the flux change that it induces within a receiver coil. It is then amplified and shaped into a digit pulse of standard amplitude. The schematic arrangement is shown in fig. 1.13, which also shows the principal waveforms in the circuit. The nickel line is made up from six strips of pure nickel. The portions encircled by the coils are annealed to ensure the maximum magnetostrictive effect; the rest of the line is not annealed, because hard drawn strip has better transmission properties. The ends are embedded in cones of rubbery plastic to absorb back propagation and prevent reflection.

35. The circuit of the nickel-line portion of the package is shown in fig. 1.14. Entry is by twin AND gates with a clocked output, similar to the entry to the twin-delay element (package type 1). The clocked digits are applied to the grid of V3*a*, and cause a pulse of anode current and hence a thrust or tension in the nickel (according to the initial conditions). Notice that any stress induced in the nickel is immediately followed by a restoring stress in the opposite sense. A biasing field is applied by a permanent magnet to the portion of the line under the coil to give the maximum input efficiency.

36. The stress wave is picked up at the remote end of the line by a receiving coil built, for convenience, to the same specification as the transmitting coil. There is a permanent biasing field at this end of the line as well to align the magnetic domains so that all the elementary changes of flux are additive. The amplitude of the e.m.f. across the receiving coil is about 1V peak; this signal is amplified in V1*a* and V1*b* in cascade to give a signal of about 30V peak. A proportion of the voltage produced at the cathode of V1*b* by R22 is fed back to the grid of V1*a* to give some stabilisation against valve aging, the amount of feedback, and hence the gain, being controlled by RV1. In an earlier mark of the package, the whole cathode voltage is fed back, R22 being the variable gain control.

37. The shaper is identical, except for the input circuit and the output cathode loading, with the delay circuit in packages of types 1 and 2. The length of the nickel line must therefore be adjusted to give a delay one digit-time less than the total delay required from the unit. The signal at the anode of V1*b* is clipped by MR17 and by cut-off action in V2*a* to give a clock-like pulse. MR16, R24 and R25 form a bias chain holding the grid of V2*a* at a mean potential of -15V; spurious signals and noise at the anode of V1*b* reach only about 5V above the mean level, and are consequently well below the cut-off level of V2*a*. The effect of MR16 and R24 is to make the impedance of the circuit between C7 and V2*a* practically linear. There is no 'mix' output from the shaper, as the first operation on the output of the line will usually be some form of address gating. Test sockets are provided at the output of the amplifier and the output of the shaper.

38. The timing of the clock-like input to the shaper depends on line length. If it is coincident with 'clock', and therefore in the optimum timing relative to the 'strobing' reset pulse, the output will be a standard digit pulse. If it is too far advanced on 'clock', the output pulse will be preceded by a spike: if it is retarded, the output pulse will be narrower than standard. A rise in temperature of 20°C will increase the length of a 41-digit line by rather more than one tenth of a digit-time; but the shaper output should still be a perfectly acceptable digit pulse. The shaper will in fact operate on pulses delayed as much as half a digit-time on 'clock'; but whether the result can be tolerated depends on the use that is to be made of it in the machine. The effective line length can be adjusted by means of an 8BA screw projecting through the valve platform, which will move the transmitter coil through a distance equivalent to half a digit time (17 turns of the screw).

Special Inverter

39. The last triode on the package, V3*b* is used as an inverter for clearing store lines. Fig. 1.15 shows the circuit. To provide the correct voltage levels with enough drive power, its output must be AC-coupled and DC-restored; moreover, to ensure that there is a fixed base level to restore to, the input to the inverter must be 'clocked', leaving only two AND-gate inputs for control signals. The output is limited in the negative direction to -10V by MR5, and to a few volts positive by MR4 and R5. The inverter output is slightly delayed on its input, and therefore on 'clock'; consequently the AND operation with digit pulses and with 'clock' at the input to the line circuit causes a small spike, as shown in fig. 1.15, which, however, is not large enough to produce an appreciable signal in the line.

40. The component layout and wiring for package type 6 is shown in fig. 1.16. The nickel line is formed into a smooth double loop, and is supported in a sleeve of expanded polythene to reduce attenuation. The sleeve is fixed to a separate plastic plate, which is bolted through spacers to the main plate and can therefore easily be changed if necessary. The length-adjusting screw projects through the valve platform so that it is accessible when the package is fitted in a cabinet. The gain control, RV1, is fixed to the main plate, and is accessible through a hole in the valve platform. (The gain control on earlier models is mounted on the side of the package, which must be removed from the cabinet to adjust the gain). The digit length of the whole element (line plus digit delay) is engraved on the end of the adjusting screw, and also appears in the serial number printed on the package.

41. Loading Data

Nickel line

(i)	Standing current	1.0 mA
(ii)	Bleeder current	1.1 mA
(iii)	Fixed load	3.3 mA
(iv)	Loose load, pin 20	2.5 mA

Inverter

Bleeder current (including leakage through clocking crystal)	1.1 mA

N.B. The only gates that may be driven by this inverter are those of the nickel line on the same package, to which it is correctly matched.

CATHODE-FOLLOWERS (TYPE 8)

42. Fig. 1.17 shows the circuits on package type 8. Elements 1, 2 and 3 are simple cathode-followers with direct outputs and corresponding test points. Elements 4 and 5 are similar, but with the alternative of a 'mix' output. Test points 4 and 5 are connected either to the direct output or to the 'mix' output according to the back wiring. The entry to element 6 is a four-input OR gate; this element has only a direct output. Fig. 1.18 shows the package layout.

43. Loading Data

(i)	Standing current	2.0 mA
(ii)	Bleeder current zero	
(iii)	Fixed loads	
	Elements 1, 2, 3, 6,	5.8 mA
	Elements 4, 5,	2.5 mA

(iv) Loose loads

Pin number	Load value
10	1.0 mA
15	2.5
20	2.5
24	1.0

(v) The effect of attaching a cathode-follower or OR gate to an output is to drain away an extra 0.3 mA.

CHAPTER II

INPUT AND OUTPUT

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CHAPTER II

INPUT AND OUTPUT

NUMBER GENERATOR (TYPE 7)

1. The number-generator package has been designed to enable serial digit trains to be produced from DC or low-frequency signals (i.e. handkey settings or tape-reader outputs) by gating with standard timing pulses. The package circuit and layout are shown in figs. 2.1 and 2.2. Elements 1, 3, 4 and 6 are simple cathode-followers with low tail resistance, which are intended primarily for use in the timing-pulse lines. Elements 2 and 5 are the number-generators proper: cathode-followers fed from the mixed outputs of three two-input AND gates. As numbers with more than three digits will normally be generated in a particular application, only a 'mix' output is provided.

2. Any one of the AND gates may have to supply the full pull-up current through the grid potentiometer as well as the drain through the back conductance of the other two OR crystals; consequently the AND-bleed resistor is low (150K). This imposes in turn a heavy loading in the 'down' condition on the driving circuit; hence the provision of cathode-followers with low tail resistance on the same package. The control inputs, pins 6(27), 8(25) and 13(27) are capacitively coupled to earth and tied through 330K resistors to the -150V rail. This arrangement enables a 'nought' to be fed into the system by leaving the input terminal on open circuit, e.g. by leaving a handkey open. The bleed to -150V ensures that the control crystal (MR2, say) is permanently conducting; the corresponding timing-pulse crystal (MR3) then rectifies the timing-pulse train, the result being integrated by C1 to produce a steady level of -10V at the control input.

3. Loading Data

Number Generator

(i) Standing current 2.5 mA
(ii) Bleeder current 2.0 mA (including leakage through signal crystal)
(iii) Fixed load 2.5 mA
(iv) Loose loads

Pin Number	Load value
15	2.5 mA
20	2.5

N.B. Loose loads are for the 'mix' only. The fixed load takes only the valve standing current, leaving the loose loads as an OR bleed to take the hold-down current for succeeding gates.

Cathode-followers

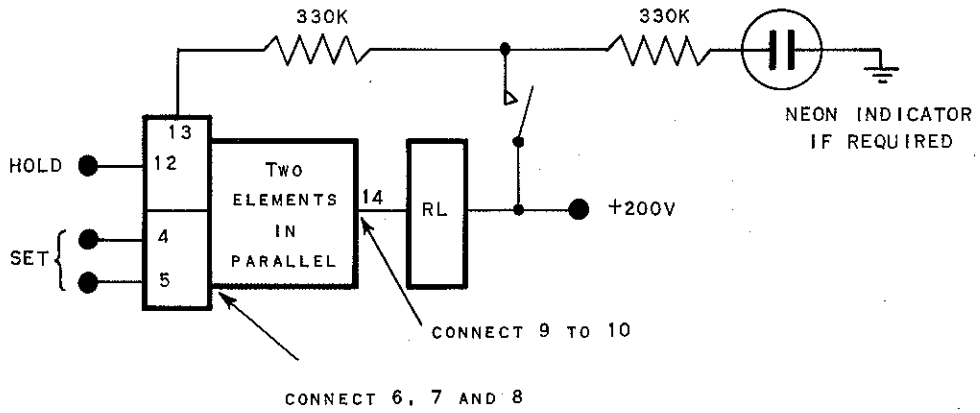
(i) Standing current 2.0 mA (but see below)
(ii) Fixed load 5.7 mA
(iii) The effect of attaching a cathode-follower to an output is to drain away an extra 0.3 mA.

N.B. When a cathode-follower is driving two number-generator gates, the total bleeder current is 4.0 mA. As the tail resistor accepts only 5.7 mA, an upper limit of 1.7 mA is set on the valve standing current. The standing-current allowance is 2.0 mA, so there may be a slight rise in the 'down' level; but this will eventually be offset owing to the high standing-current allowance of the number-generator valve.

OUTPUT ONE (TYPE 9)

4. The circuit of the Output One package is shown in fig. 2.3 and the component layout in fig. 2.4. The package contains six triode amplifiers (half 12AT7), which can be used to drive neon-indicator lamps and low-current relays from digit-pulse waveforms. The package also contains two crystal gating networks for use as a setting and resetting device with relays. Neon lamps are connected between the anode pin of the element and the HT rail, in series with a suitable current-limiting resistor. To preserve the operating life of the valves, the anode current should not be allowed to exceed about 10 mA.

5. The circuits were originally developed for use with STC relays, type 4184GE, for which two elements must be used in parallel. The recommended arrangement for the elements 1 and 2 is as shown below.



The relay coil is connected between the anodes and the HT rail in series with the current-limiting resistors R7 and R8 (R15 and R16) on the package. A pair of hold-on contacts on the relay is used to connect a 330K bleeder resistor between HT and the 'reset' side of the crystal network. The device is set by coincidence between the inputs to pins 4 and 5 (24 and 25); it is recommended that coincidence persist for at least 15 milliseconds to allow for the mechanical inertia of the relay. The device

is reset when the signal at pin 12 (17) falls to -10V, cutting the valve off. The capacitor between the gate output and earth limits the rate of rise or fall of grid potential, and hence the rate at which current builds up in the relay coil, and the size of the resultant overswing.

6. Loading Data

The gate requires a bleeder current of 1.0 mA. When used for operating a neon lamp alone, the load on the driving staticiser is negligible.

OUTPUT TWO (TYPE 10)

7. The Output Two package, shown in figs. 2.5 and 2.6, contains three 6CH6 pentodes to supply some 40 mA each for operating tape-punch equipment from logical signals. The load is connected between the anode of the valve and the 300V HT rail. An integrating circuit between anode and earth limits the rate of current decay in an inductive load, and hence the overswing amplitude.

8. Loading Data

This element imposes no load on a 'down' signal; but a grid current of 2.0 mA must be allowed for when the input signal is 'up'.

THYRATRON OUTPUT (TYPE 26)

9. This package has been designed as a high-current output unit, e.g. to operate card-punch equipment. It operates from a single digit pulse that may have an amplitude as low as the γ- level. The circuit and layout are shown in fig. 2.7 and 2.8. There are two elements to a package, each consisting of an EN91 thyratron triggered from one half of a double triode, which is controlled by a four-input AND gate. One of the AND-gate inputs is used for 'clock'; the reason for this is to eliminate spurious 'spikes' produced by the logic, which might trigger the thyratron. The output of the AND gate, which is not large enough to operate the thyratron satisfactorily, is amplified in the triode. The thyratron is triggered, of course, on the rising edge of the triode output, which is coincident with the back edge of 'clock'. The triggering pulse is lengthened by the action of the coupling capacitor; this charges through the crystals during 'clock', with a time constant approximately equal to the width of 'clock', 1.5μ sec. At the end of 'clock' the anode potential of the triode, and hence the grid potential of the thyratron, rises by about 100V, the charge on the capacitor leaking away slowly thereafter with time constant of the order of 25μ sec.

10. The thyratron is rated for a maximum peak anode voltage of 650V forward and 1.3KV inverse, and for a maximum cathode current of 500 mA peak and 100 mA average over not less than 30 seconds. The anode resistor is chosen to keep the peak anode current within the rated value, and implies a maximum supply potential of 145V. The

capacitor between the output points is intended to limit the rate of change of output voltage, and thereby to reduce any interference that might be caused by pick-up from the output cable. Provision must be made for switching the anode supply externally to extinguish the thyratron. Moreover suitable interlocks must be provided to ensure that the anode supply is not applied until the heaters have been on for at least ten seconds. The reason for connecting the cathodes to output pins is to enable the current-return line for either valve to be placed, if required, in the same cableform as the output line.

11. Loading Data

The bleeder current for the gate, including an allowance for leakage through the 'clock' crystal is 0.85 mA.

C H A P T E R I I I

TIME STANDARDISATION

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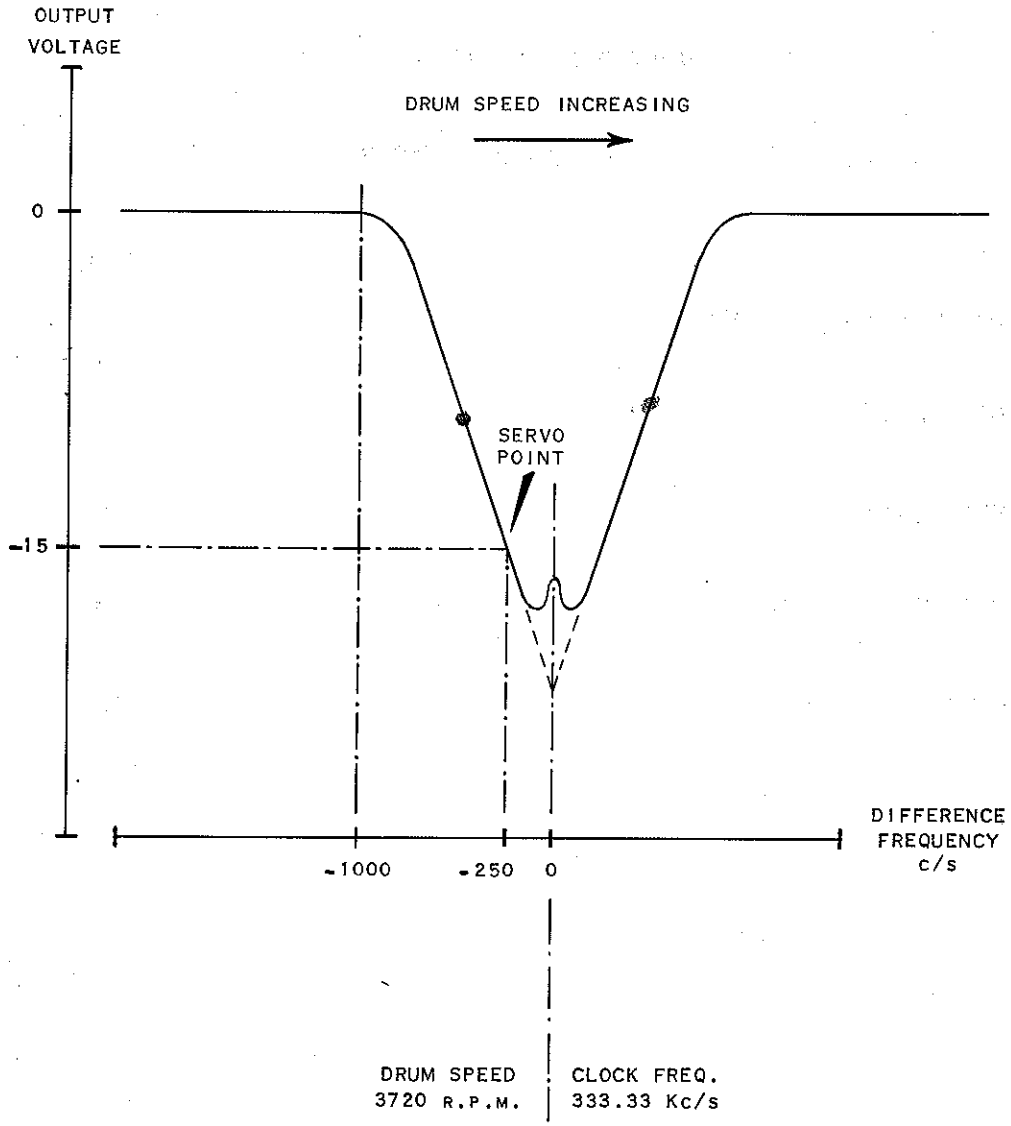

DISCRIMINATOR CHARACTERISTIC

CHAPTER III

TIME STANDARDISATION

1. A set of packages has been developed to generate the 'clock' and 'reset' waveforms required for standardising the digit-pulse timing. In a simple system, the waveforms can be derived from a crystal oscillator, package type 11, shaped in package type 12 and fed to the waveform-output package, type 13. The shaper package can be arranged, by suitable back-wiring connections, to give either a 'clock' output or a 'reset' output. The back wiring of the output package also depends on the waveform for which it is used.

2. Where 'clock' has to be synchronised with the rate of rotation of a magnetic drum, the arrangement shown schematically in fig. 3.1 is used. The crystal oscillator is now a reference against which the drum speed can be servo-controlled. A sine wave is picked up from the clock track of the drum, boosted to 33V peak-to-peak in the clock amplifier, package type 20, and fed, together with the output of the crystal oscillator, to the discriminator package, type 21, whose output is used for servo-control. The output of the clock amplifier is also shaped and fed to the output packages; alternatively the oscillator can be switched direct to the shapers for testing without a drum.

CRYSTAL OSCILLATOR (TYPE 11)

3. The oscillator circuit is shown in fig. 3.2, and the package lay-out in fig. 3.3. The crystal is in effect connected between anode and cathode of the oscillator valve proper, V1*a*, and it is operating in a series mode. V1*b* is used as a cathode-follower in the crystal-current path, thereby reducing the direct voltage across the crystal and the effect of circuit parameters on the operating frequency. The anode circuit of V1*a* is capacitive, the capacitor and resistor having the same impedance at 333.33 Kc/s, the natural frequency of the crystal; thus the harmonic content of the anode waveform is very much attenuated. The grid is capacitively coupled to the positive HT line, giving a pull-up to start the oscillator when the HT supplies are switched on. The output stage, V2, is a cathode-follower. As it is fed from the anode of V1*b*, the operating frequency of the oscillator is practically independent of output loading. The output is a sine wave of 65V to 70V peak-to-peak, with its mean level at about +8V.

SHAPER (TYPE 12)

4. This accepts a 65V sine wave from the oscillator or, from the clock amplifier, a partially squared waveform of 33V peak-to-peak that may be thought of as the centre portion of a sine wave of the same amplitude as the oscillator output. The circuit is shown in fig. 3.4 and the layout in fig. 3.5. The input network is symmetrical with respect to the input point; consequently the waveform on the grid side of the input

capacitor is symmetrical about earth. This waveform is limited positively by crystal MR2 and negatively by cut-off in V1; so the anode waveform of V1 is a square wave sliced very nearly at the mean level of the sine wave. A catching crystal, MR3, in the cathode circuit of V1 protects crystal MR2 against excessive grid current in the event of valve failure or an open-circuited anode load.

5. The amplitude of the signal at the anode of V1 is about 70V. The grid of V2 is biased to -10V, and positive excursions above earth are limited by MR4. When the package is used as a 'clock' shaper, pins 19 and 31 are connected together so that the anode network is shorted by capacitor C7, leaving only a resistive load of 2.2K (R12). V2 then acts simply as a switching valve, giving an output amplitude of 110V peak-to-peak. The cathode is caught negatively at earth, and the amplitude of the signal on it, i.e. at monitor point X, is 8.5V.

6. When the package is used for shaping 'reset', pin 31 is left floating and pin 19 is earthed so that capacitor C7 becomes a decoupling by-pass. The falling edge of the square wave at V2 grid, cutting the valve off, sets up a 'ring' in C6 and L1, which is damped out by the crystal network after the positive half cycle. Inductor L1 is dust-cored. It is mounted behind the valve platform, with the core accessible from the front when the package is mounted in the rack. The width of the reset pulse can therefore be adjusted with the package in situ; but the inductance of L1 should be adjusted beforehand to 1/2 mH, when the correct pulse width of 0.6μ sec. will be produced. The pulse amplitude at the anode of V2 is 155V (positive-going). The waveform at the cathode (monitor point X) is the same as for clock shaping, a square wave of amplitude 8.5V. The attenuated negative overshoot appears after the ring on the anode waveform, and also a small negative 'blip' coincident with the rising edge of the input. These are removed by clipping in the last stage.

7. V3 is a cathode-follower, whose grid is returned (pin 10) to +13V for 'clock' or -20V for 'reset'. The catching crystals, MR16 and MR17, at the cathode remove the spurious variations from the bottom of the 'reset' waveform, leaving a positive pulse of amplitude 135V off load or 130V on full load. The 'clock' output, which is also caught at earth, has an amplitude of 80V peak-to-peak. The rising edges of 'clock' and 'reset' have the same timing at this point; but there is an overall inversion in the waveform output package, so it is the *falling* edges of 'clock' and 'reset' that are coincident throughout the computer.

WAVEFORM OUTPUT (TYPE 13)

8. The circuit of this package is shown in fig. 3.6, and the layout in fig. 3.7. It comprises a pentode cathode-follower driving two pentodes in parallel. The output transformer has two primary windings one in the anode circuit, the other in the cathode circuit, of the valve pair. These two primaries give the same number of ampere-turns, necessitating a turn ratio of 40 (cathode) to 47 (anode) between the two. There are four secondary windings, each with 8 turns to the 40 or 47 turns on the primaries. The secondaries are connected in parallel pairs to four output pins, which are series-connected for 'reset' or parallel-connected for 'clock'.

9. The 'clock' and 'reset' waveforms are distributed on coaxial cable. The recommended output connections are as follows:

Clock

pin 21 to 25 to 20 (test point) to inner of coax.
pin 23 to 27 to outer of coax.

Reset

pin 23 to 25
pin 21 to 20 (test point) to inner of coax.
pin 27 to outer of coax.

The bias (-4V for 'clock' and +13V for 'reset') is connected to the outer conductor of the cable at the receiving end, where there is also a decoupling capacitor to earth. The 'clock' output is then a square wave extending from +2V to -10V, and the 'reset' output is a negative 0.6μ sec. pulse extending from +18V to between -20V and -25V. The output package has a rated output of 1A peak, giving sufficient 'clock' power to drive some 250, or sufficient 'reset' power to drive some 70, delay elements or store lines. The distributing cables are terminated by anti-ring resistors, whose valves depend on the loading and cable length.

CLOCK AMPLIFIER (TYPE 20)

10. The 'clock' sine wave from the drum reading head should be nearly 2 mV peak-to-peak. The purpose of the clock amplifier, which is shown in figs. 3.8 and 3.9, is to boost this to a level that will operate the computer satisfactorily. The lead from the reading head is a screened pair, and the signal is fed to the amplifier through an approximately tuned transformer giving a step up of 20:1. The first amplifying stage has a voltage gain of 20, a potentiometer between the anode and the -150V line providing an automatic grid bias of -2V.

11. The gain of the tuned second stage is about 40. The purpose of the tuning is not only to increase the gain but also to make it possible to vary the phase, and hence the timing, of the output, and thus enable timing margins to be set for testing the drum-read circuits. Two trimmers are necessary to give the required timing range; these are mounted on the side of the package, which must therefore be fitted at the end of a row so that the trimmers are accessible from the drum cavity. They should be set finally to give maximum signal at test point X, which is the latest point where the form of the 'clock' sine wave can be inspected. This point is connected to the valve through a 2.2pF capacitor to reduce the load imposed by the measuring device, a 1K resistor giving a standard internal load for measurement.

12. The output stage, which is a cathode-follower, is preceded by a pair of limiting diodes to guard against asymmetric squaring in the valve, the ultimate requirement being a square 'clock' waveform sliced symmetrically from the original sine wave. A monitor point (Z) is connected to the package output, where the partially squared signal should have an amplitude of nearly 33V peak-to-peak and a mean level of +1.5V.

DISCRIMINATOR (TYPE 21)

13. The discriminator is shown in figs 3.10 and 3.11. The outputs of the crystal oscillator and clock amplifier are applied to an AND gate, which, by virtue of its non-linear impedance, produces the required difference frequency. This is applied to the grid of V1, the higher frequencies being filtered out by the stray interelectrode capacitance in conjunction with the 1M grid resistor. Because of cut-off in V1 and grid-current limiting, the anode waveform (test point A) is a square wave of unity mark-space ratio swinging from +25V to +240V.

14. The frequency-discriminating circuit consists of capacitor C3 and the network in the grid circuit of V2*a*. This arrangement is known as a 'diode pump' circuit. MR6 conducts during the positive swings at the anode of V1, and restores the potential on the grid side of C3 to that at the cathode of V2*a*, the charge on C3 being shared with C6 in the process. During the negative swings of the signal, the charge on C3 is replaced from C5, which is replenished in turn by leakage through R12 during the positive half cycle. Hence the 'pump' analogy: C3 may be thought of as drawing charge from C5 through a one-way device, an amount of charge proportional to the signal amplitude being transferred each cycle; the drop in the voltage level at the grid of V2*a* is then proportional to this and to the frequency of 'pumping'. The amplitude of the signal at the anode of V1 is 215V peak-to-peak; hence the charge transferred each cycle is:

$$215 \times 0.0022 \times 10^{-6} \text{ coulombs}$$

This must be replaced on C5 every cycle by leakage through R12. The mean current through R12 is then

$$215 \times 0.0022 \times 10^{-6} \times f \text{ amps}$$

when f is the beat frequency. This implies a potential drop across R12 of

$$215 \times 0.0022 \times 10^{-6} \times f \times 220 \times 10^{3}$$

$$= 0.102f \text{ volts.}$$

The discriminator therefore has a theoretical response of approximately 0.1 volt per cycle. It should be noted that MR6 must be returned to the cathode of V2*a* rather than to earth, so that the pump can make use of the full amplitude of the square wave.

15. So far it has been assumed that the discriminator is not amplitude-sensitive, which will be true as long as the amplitude of the beat signal is great enough to cause appreciable limiting in V1. The response of the clock amplifier, however, is flat over a small range only; consequently the beat amplitude will fall off at high difference frequencies and reduce the charge transferred each 'pumping' cycle. If resistor R12 were returned to a constant potential, there would be a rise in potential at V2*a* grid, and a fall in the package output level, outside the discriminator 'dip'. The result would be no field current at low drum speeds, when a high field current would be desirable for run-up, and, moreover, a second falling portion on the discriminator

characteristic, where the system would be stable with the drum-clock frequency *above* that of the crystal oscillator.

16. To make the package characteristic level except over the discrimination dip, the signal at the anode of V1 is peak-level rectified by MR3 and MR4 and applied to V2*b* to control the return potential for the leak resistor, R12; thus the reduced 'pumping' due to falling amplitude is compensated by a falling potential at the cathode of V2*b*. Over the normal working range, the cathode potential of V2*b* (monitor point K) is about 70V, with a ripple of amplitude about 2V. The sockets marked +300, B and E are not primarily for monitoring; they are provided to enable a variable potentiometer, the drum-speed adjuster, to be plugged into the package in situ so that the potential at V2*b* cathode, and hence the running speed of the drum, can be varied during the process of writing an initial 'clock' track.

17. The frequency-dependent signal at the cathode of V2*a* is inverted by a see-saw circuit to provide a control voltage for the drum-motor supply. This voltage is actually applied to a battery of valves that control the field current of the generator supplying power to the drum motor; (see Volume 3, Chapter III) thus a rise in the output voltage of the package increases the drum speed and hence the drum-clock frequency. A rise in the output voltage of the package, i.e. a fall in potential at the cathode of V2*a*, implies an increasing difference frequency; consequently the system is stable, an increasing drum speed opposing an increasing difference frequency, only so long as the drum-clock frequency is *below* that of the crystal oscillator. The overall characteristic of the discriminator package is shown at the beginning of this chapter.

18. The package output is limited positively at a potential determined by the connection to pin 17. This will normally be earth, though it may be decreased to -10V if the drum is driven by a motor with a high-resistance rotor. It is advisable to introduce some 'phase advance' into the system to improve its response; this is done by connecting pins 18 and 20 together to put some capacitance across the input arm of the see-saw. Pins 28 and 30 can be connected to a neon lamp to give an indication when the drum has reached the correct running speed. The lamp will light when the anode potential of V3 falls in the discrimination dip; but, as V3 never approaches cut-off, it will not strike in the reverse direction unless there is a circuit fault.

C H A P T E R I V

DRUM STORAGE

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CHAPTER IV

DRUM STORAGE

1. The packages described in this chapter have been developed for writing and reading at a digit rate of 6μ sec. They are used with recording heads having a specified minimum inductance of 25μH. These are wound on ferroxcube cores with a gap width of 0.5 thou., and are mounted with a mean separation of 1.5 thou. from the drum surface. A writing current of about one amp is required, and they give a signal of about 1 mV r.m.s. for reading. The heads are supplied in stacks of ten, of which generally only eight are used in the present installation.

2. As the digit rate for storage is half that for computing, the digits in a word are written alternately on a pair of tracks. The magnetisation pattern is equivalent to a phase modulation of the original pulse waveform, a series of 'ones' and a series of 'noughts' giving the same magnetic pattern (saturation for 3μ sec. in one direction followed by saturation for 3μ sec. in the opposite direction) but with a phase difference of 180°. Logical circuits have been designed for separating alternate digits of the information to be recorded, for producing the required phase-modulated signals, and for splitting the phases of these to feed the push-pull writing amplifiers. Signals read from the drum are amplified and then strobed every 3μ sec. (to eliminate timing variations due to changes in amplitude) and shaped to the normal digit form. Gating with standard timing pulses in alternate digit intervals then reconstitutes the two halves of the original information.

3. The packages are intended for use with a drum carrying forty track pairs, which are considered for the purposes of selection as a matrix of five 'columns' and eight 'rows'. The row-selection and column-selection signals derived from the logical circuits have opposite polarities, the track selected being the one for which the level of the column-selection signal algebraically exceeds that of the row-selection signal. The arrangement for a single track is shown in fig. 4.1. The recording head is connected to a transformer in the write-read switch (package type 16), and the 'read' signal can pass to the read amplifier only if the outputs of both read-switch controls (type 19) are in the 'on' condition. There is one pair of write-read switches to each column; consequently there are five pairs of packages of this type in the matrix, each carrying eight transformers. There are five read-switch controls for column selection, each controlling a pair of write-read switches, and eight for row selection, each controlling one transformer in each write-read switch.

4. The transformers in the write-read switch carry a third winding, which is used as an anode load for the output valves of the write drive (package type 14). Column selection for writing is carried out at low level, at the input to the write-drive package. Row selection is carried out by high-level switching, HT power being supplied from the write-switch control through the appropriate transformer winding to the selected write-drive package. There are therefore eight write-switch controls in the

installation, each supplying one transformer in every write-read switch. In addition, there are two packages of this type connected to operate as a stabilised +100V supply. According to the matrix, there should be one write-drive package to each write-read switch; but one column in the present installation is treated as an isolated part of the store that can be read from but not overwritten: consequently there are only eight write-drive packages, two of which must be transferred temporarily to another rack position for writing the permanent record.

5. Writing is possible only if the 'inhibit write' pins on the socket of the write-drive package are connected together, e.g. by means of a relay. This facility is provided to protect the drum record in the event of a power-supply failure. The 'suppress write' signal applied to the write-switch control is derived from the logical circuits. It should be in the 'suppress' condition during reading, to prevent noise breakthrough from the selected write-drive package.

N.B. The drum-store packages are not designed to operate on marginal HT supplies.

WRITE-SWITCH CONTROL (TYPE 14)

6. The write-switch control is shown in figs. 4.2 and 4.3. When the package is used for control, the row-selection waveform is applied to pin 4, and the 'suppress write' signal to pin 5, pins 12 and 13 being connected together. The two signals therefore undergo an OR operation followed by inversion in V1. The negative-going significance of the two inputs may be taken to imply that they are both inverted positive-significance signals; hence by the logical identity

$$\sim (a \vee \sim b) \equiv a \,\&\, b$$

the anode potential of V1 is at its highest level when the appropriate row has been selected *and* the 'suppress write' signal is in the permissive condition. The 'permit' level of the input is -10V, and crystal MR3 catches the cathode of V1 at earth, pin 15 being disconnected; consequently V1 is cut off when the circuit is in the 'on' condition. Its anode is then at +200V, and falls below +80V when either input is positive. Capacitor C2 between the OR gate and the grid of V1 provides some smoothing, the two inputs normally being derived from inverters.

7. The anode waveform of V1 is fed to the grids of V2 and V3, which are connected in parallel and fed from the +300V HT line (pin 32). The output is taken from pin 29, which is connected to the cathodes of these valves. The output level is +160V in the 'on' condition, and is caught negatively at +100V when the circuit is in the 'off' condition, the +100V supply being connected to pin 30 for this purpose. Pin 14 is disconnected when the circuit is used as a switch control.

+100V Supply

8. When the package is used as a stabilised source of +100V, pins 12 and 30 are left floating, pins 13 and 14 are connected together, pin 15 is connected to earth (pin 16), and the anodes of V2 and V3 are fed from the +200V supply (pins 31 and 32 being connected together). V2 and V3 then control the output current according to the

anode level of V1. The grid of V1 is fed through package pins 13 and 14 from a potentiometer chain between the output point and the -150V line, which therefore supplies the reference level. Stabilisation is within ±3% for currents up to 100 mA.

READ STROBE (TYPE 15)

9. The read-strobe package is shown in figs. 4.4 and 4.5. There are two identical elements to a package. The input (pin 4 or 28) which comes from the read amplifier, is limited between +13V and -20V and applied to a pentode cathode-follower driving a crystal-diode bridge. 'reset' is used for strobing, a transformer being used to invert the waveform for feeding the positive end of the bridge. Between strobe pulses, MR9 and MR10 are conducting; so the top end of the bridge will be rather below -10V, and the bottom end will be at the positive level of reset, +18V. During the strobing, MR9 and MR10 are cut off, and the bridge crystals become conducting, allowing the grid of V2 to be pulled up if the cathode of V1 is positive. A 100pF capacitor is provided to maintain the potential at the grid of V2 from the time that a positive pulse has been strobed until the next strobe pulse. The result is a digit-like waveform at the cathode of V2, with its peak level at +13V and its base level caught at -10V. Notice that there are two crystal in series in each of the output arms of the bridge to reduce changes in potential across the capacitor due to back conduction between strobe pulses. V2 has fixed loads of 1.0 mA and both direct and 'mix' outputs. Loose loads of 1.7 mA and 3.3 mA are provided for each element.

WRITE-READ SWITCH (TYPE 16)

10. The write-read switch is shown in figs. 4.6 and 4.7. This package differs in construction from the others in having six eight-pin moulded plugs instead of four. The extra two plugs are mounted at the right-hand side of the plate (as seen from the front of the cabinet) so that their pins are in line with the odd-numbered pins on the other plugs. The extra pins are referred to with odd numbers 1*a* to 31*a*. The package contains eight head transformers, constituting one column of the matrix, and a pre-amplifier for feeding the read amplifier.

Writing

11. Consider transformer TR1. The head is connected to one winding of this transformer via pins 17 and 18. Another winding is coupled through crystals to pins 7 and 9, which are connected to the anodes of the push-pull amplifier in the write-drive package for the appropriate column. HT power at 160V for this amplifier is supplied, via pin 1*a* and the centre tap of the transformer winding, from the write-switch control when the appropriate row is selected; the outputs of the other write-switch controls (pins 3*a*, 5*a*, 7*a* etc.) will then be at +100V, isolating the other transformers in the column by cutting off the crystal diodes. Column-selection for writing is done in the write-drive package (see paragraph 14).

Reading

12. A particular head is selected for reading when the signal from the column read-switch control is negative. The switching is done by a crystal-diode bridge; the

column-selection signal, which is common to all the switches on the package, is applied to pin 14, and the row-selection signal, for transformer TR1, to pin 17*a*. When transformer TR1 is selected, crystals MR5 and MR6 are forward conducting, and the signal is fed through 10K resistors to the input of the pre-amplifier: otherwise MR7 and MR8 are forward-conducting and place a low impedance across the transformer output, while the high back resistance of MR5 and MR6 prevents an appreciable signal from being developed.

13. The purpose of the pre-amplifier is to present the read amplifier with a signal amplitude and output impedance that are substantially the same as would be obtained by direct connection to the head. This enables the same read-amplifier circuit to be used for information tracks as for address tracks, where there is no switching. The pre-amplifier valve has a voltage gain of 8; the transformer preceding it gives a voltage step-up of 2:1, and it is coupled to pins 13 and 15, and hence to the read amplifier, by a matching transformer giving a voltage step-down of 10:1. Notice that crystal MR65 isolates the valve from the output transformer except when the column-selection signal is positive. This is necessary, because five write-read switches are connected in parallel to one read amplifier, to prevent a high current load from being imposed on the selected package by the unselected packages.

WRITE DRIVE (TYPE 17)

14. The write-drive package is shown in figs. 4.8 and 4.9. The signals from the logical phase splitter are fed to pins 13 and 15 and undergo an AND operation with the logical column-selection signal, which is applied to pin 14. Test points are provided so that the results of this operation can be studied. V1 gives enough gain to ensure that there is appreciable limiting at the inputs to the drive valves, V2 and V3, when the package input is a β-level signal. Its cathode is caught at earth by MR3 to ensure that both halves of the valve are cut off when there is no input signal (in orders other than 'write' orders) or when the particular column is not selected.

15. The double-ended signal from transformer TR1 is fed to the grids of V2 and V3. The grid waveforms are limited positively at earth, and the negative excursions are large enough to cut the two valves off in turn. The anode load is the selected transformer in the write-read switch, which is connected across pins 7 and 9. One or other of these transformers will always be in the selected condition, i.e. with +160V HT applied from the write-switch control, even if the particular column is not selected, provided that the 'suppress write' signal is not positive. The anode waveforms (test points Z1 and Z2) should swing between +160V (valve cut off) and +100V, the catch at +100V (pin 4) being provided to prevent breakthrough to the unselected transformers, which will also be at +100V.

16. The cathode circuit of V2 and V3 must be considered in relation to the whole installation. As one fifth of the drum store is to be isolated, there will be only four write-drive packages for the odd tracks and four for the even tracks. The arrangement for the odd tracks is the same as for the even tracks: pin 10 on each package is connected to pin 10 on the other three and also to one contact on the 'inhibit write' relay; pin 11 of three of the four packages is connected to the adjacent contact on

the relay, pin 11 of the fourth package being left floating. The relay contacts are closed during normal operation; consequently the four output stages have a common cathode load of about 330 ohms (three R7 in parallel). In the event of a power-supply failure, the relay contacts open and an extra 33K (three R10 in parallel) is added in the cathode circuit to impose a paralysing bias on the valves. Crystals MR12 and MR13, of which there will be four pairs in parallel, catch the cathodes at earth and keep the valves cut off when there is no signal input (in orders other than 'write' orders and between words in 'write' orders).

READ AMPLIFIER (TYPE 18)

17. The read amplifier (figs 4.10 and 4.11) is designed to accept pulses of about 1 mV peak-to-peak, to square and delay then to bring them over the strobe pulse, and to provide a signal of about 32V peak-to-peak for the read-strobe package. The first stage of amplification gives a gain sufficient to cause limiting in the crystal circuit following it. The anode of V1 is well decoupled and is returned to a different HT supply from the valves on either side of it. The crystal circuit limits at earth and -2V, giving a signal of 2V peak-to-peak, centred on 1V, at monitor point X.

18. The second stage of amplification, V2, has a gain of about 30. It feeds the L-C delay section, which is arranged to pad out the delay necessarily involved in writing and reading to an odd number of half digit-times. To give a little extra delay, capacitor C8 can be brought into circuit by connecting pin 15 to earth (pin 16); this would be done to accommodate differences in wiring capacitance, or to compensate the stray capacitance involved in track switching, which does not appear in the address-track chain. The output of the delay section is again crystal-limited and amplified in V3 to give an output signal (test point Z) of about 32V peak-to-peak. The delay between V2 and V3 is about 1/3 μ sec.

READ-SWITCH CONTROL (TYPE 19)

19. The read-switch control (figs. 4.12 and 4.13) is used to give the low-level switching signals required by the write-read switch for column selection and row selection during reading. It also provides a high degree of smoothing to remove inter-digit spikes produced by the logical circuits, which might otherwise impair the working of the switch. The package comprises eight identical elements, of which only five are available for column-switch control.

20. For column switching, pin 5 is connected to the +100V supply (package type 14) to provide pull-up for the output when the input is in the 'up' (selected) condition. Pin 9 is connected to a bias supply at +1.5V, and pin 7 to a supply at -3.5V; as there will be a potential drop of about 0.5V across the limiting crystals, the output levels for column switching are about +2V (selected) and -4V (unselected). The signals for row-switching are negative during selection; pin 5 is disconnected for row control, the -150V connection to pin 11 providing pull-down when the input is in the down (selected) condition. Pin 9 is connected to +4.5V and pin 7 to earth; the output levels, with a potential drop of 0.5V assumed across the limiting crystals, are then

+5V (unselected) and -1/2V (selected). It is advisable to take the *column*-selection signals to the read-switch control through the 'mix' crystals of the delays generating them, so as to allow the outputs of these delays to fall to -10V in the unselected condition; the pull-down to -150V in the read-switch control is then necessary for column selection as well as for row selection. The special bias arrangement must be capable of supplying 50 mA to each package.